the limitations of the base claim and any intervening claims.

Applicants have amended Claim 11, thereby obviating the rejection under 35 U.S.C. §112, 2nd paragraph. Claims 12, 34, 36, 40, 47 and 48 depend directly or indirectly on allowable Claim 11 and should be allowable as well. Even though the Examiner indicates that Claim 12 is withdrawn from consideration, Applicants request that the Examiner consider Claim 12 as it depends on Claim 11 which was elected.

Claims 33, 35, 37, and 38 have been rewritten to overcome the rejection under 35 U.S.C. §112, 2nd paragraph, and to include all of the limitations of Claim 10 from which they formerly depended. Thus, Claims 33, 35, 37 and 38 should be allowable.

The rejection of Claim 10 under 35 U.S.C. §103(a) over Kirk et al (U.S. 5,444,244) is respectfully traversed.

Claim 10 has been amended to claim a radius of curvature of the conic body of several to about 15 nm. Claims 39, 46 and 2-7 depend directly or indirectly on amended Claim 10. Thus, the present invention as set forth in amended Claim 10 relates to a semiconductor device, comprising:

a conic body formed on a semiconducting material substrate or a semiconducting material layer;

wherein said conic body has a radius of curvature of several to about 15 nm in the vicinity of its leading end or a diameter of about 10 nm to 30 nm in the vicinity of its leading end, and an aspect ratio of about 10 or more.

In contrast, Kirk et al discloses a conic body having a very small tip radius of less than 200 Å (Kirk et al, col. 5, lines 19-51, col. 12, line 22) and an aspect ratio of grater than 2:1 (Kirk et al, col. 12, line 21). However, there is no disclosure or suggestion of the specific sharp conic body as claimed having a radius of curvature of several to about 15 nm in the

vicinity of its leading end or a diameter of about 10 nm to 30 nm in the vicinity of its leading end, and an aspect ratio of about 10 or more. In addition, such a sharp conic body cannot be formed by the method of Kirk et al.

Therefore, the rejection of Claim 10 under 35 U.S.C. §103(a) over Kirk et al (U.S. 5,444,244) is believed to be unsustainable as the present invention is neither anticipated nor obvious and withdrawal of this rejection is respectfully requested.

The rejection of Claims 10, 11 and 33-38 under 35 U.S.C. §112, 2nd paragraph is obviated by the amendment of these Claims.

Finally, with respect to the elected species, Applicants respectfully submit that, should the elected species be found allowable, the Office should expand its search to the non-elected species of Claims 13, 19, 25 and 32 and their dependent Claims.

In addition, Applicants note that MPEP §821.04 states, "if applicant elects claims directed to the product, and a product claim is subsequently found allowable, withdrawn process claims which depend from or otherwise include all the limitations of the allowable product claim will be rejoined." Applicants respectfully submit that should the elected group be found allowable, the non-elected claims 1-9, 30 and 31 should be rejoined.

The Examiner requested Applicants to resubmit an Information Disclosure Statement, which, according to the Examiner, was filed in the above-identified application on December 14, 1999. Applicants note that the IDS was filed on October 18, 1999. The Examiner has properly considered this IDS on the record as evidenced by the signed and initialed Form 1449 which was attached to the Office Action of July 18, 2002. Thus, no further action is believed to necessary.

Applicants respectfully submit that the above-identified application is now in condition for examination on the merits, and early notice of such action is earnestly solicited.

Respectfully submitted,

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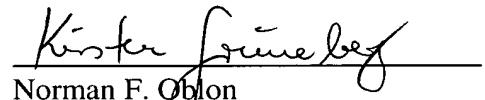

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Serial No: **09/420,524**
Amendment Filed on: **HEREWITH**

IN THE CLAIMS

--1. (Amended) A method for manufacturing a semiconductor device, comprising:

[forming an impurity precipitation region by] introducing [an] a first impurity into a predetermined position of a semiconducting material substrate or a semiconducting material layer, to obtain a semiconducting material substrate having an impurity precipitation region or a semiconducting material layer having an impurity precipitation region; and

performing high selectivity anisotropic etching of [the] said semiconducting material substrate having said impurity precipitation region or [the] of said semiconducting material layer [with the] having said impurity precipitation region [used as a micro mask], to thereby form a conic body;

wherein said impurity precipitation region is used as a micro mask during said anisotropic etching;

wherein said micro mask is a top of an etching exposure surface on which said anisotropic etching is performed and on which said conic body is formed

[the top of which is the micro mask on an etching exposure surface of the material substrate or the material layer].

2. (Amended) [A] The method for manufacturing a semiconductor device according to claim [1] 46, wherein[: the] said impurity precipitation region has an etching rate different

from that of a main component [material] of [the] said semiconducting material substrate or [the] said semiconducting material layer[,]; and

wherein said [the] impurity precipitation region is formed by thermally treating [the] said impurity introduced into [the] said predetermined position of [the] said semiconducting material substrate or [the] said semiconducting material layer, to precipitate said impurity into a crystal of the semiconducting material substrate or the semiconducting material layer.

3. (Amended) [A] The method for manufacturing a semiconductor device according to claim [1] 46, wherein [a material for of the] said semiconducting material substrate or [the] said semiconducting material layer [is] comprises silicon[,]; and

wherein [the] said impurity to be introduced is oxygen.

4. (Amended) [A] The method for manufacturing a semiconductor device according to claim [1] 46, wherein the semiconducting material substrate or the semiconducting material layer further [contains] comprises a second impurity which [is bonded] bonds to the [introduced] impurity precipitation region of said first impurity easier than to [the] a material [element] of the semiconducting material substrate or the semiconductive material layer.

5. (Amended) [A] The method for manufacturing a semiconductor device according to claim 4, wherein[: a material for] each of the semiconducting material substrate [or] and the semiconducting material layer [is] comprises silicon[,];

wherein the [introduced] first impurity is oxygen[,]; and

wherein the second impurity is boron.

6. (Amended) [A] The method for manufacturing a semiconductor device according to claim [1] 46, wherein [the process of forming the impurity precipitation region as the micro mask comprise:] said first impurity is introduced into a predetermined position of said semiconducting material substrate or said semiconducting material layer by a process

comprising:

forming an ion implantation mask, which is open at a target conic body forming region and which covers [the] a region other than the target region, on [the] a surface of the semiconducting material substrate or the semiconducting material layer[,];

[performing] ion [implantation of the] implanting said first impurity into the semiconducting material substrate or the semiconducting material layer, to obtain an implanted impurity; and

thermally treating [the] said implanted impurity to precipitate it into [the] a crystal of [the] said semiconducting material substrate or [the] said semiconducting material layer, to obtain said semiconducting material substrate having the impurity precipitation region or said semiconducting material layer having the impurity precipitation region.

7. (Amended) [A] The method for manufacturing a semiconductor device according to claim [1] 46, wherein [the process of forming the impurity precipitation region as the micro mask comprises:]said first impurity is introduced into a predetermined position of said semiconducting material substrate or said semiconducting material layer by a process comprising:

growing the semiconducting material substrate or the semiconducting material layer by an epitaxial method in a direction of a target conic body forming height[,];

adding gas containing [the] said first impurity to a material gas at a target micro mask forming height to further grow the semiconducting material substrate or the semiconducting material layer by [the] said epitaxial method[,]; and

removing an epitaxial growth layer containing the impurity while excepting the target conic body forming region.

8. (Amended) A method for manufacturing a semiconductor device, comprising:

[forming an impurity precipitation region by] introducing[an] a first impurity into a predetermined position of a semiconducting material substrate or a semiconducting material layer, to obtain a semiconducting material substrate having an impurity precipitation region or a semiconducting material layer having an impurity precipitation region;

performing high selectivity anisotropic etching of[the] said semiconducting material substrate having said impurity precipitation region or [the] of said semiconducting material layer having said [with the] impurity precipitation region [used as a micro mask], to thereby form a truncated conic body;

wherein said impurity precipitation region is used as a micro mask during said anisotropic etching;

wherein said micro mask is a top of an etching exposure surface on which said anisotropic etching is performed and on which said truncated conic body is formed [the top of which is the micro mask on an etching exposure surface of the material substrate or the material layer,]; and

exposing [the] a top surface of [the formed] said truncated conic body in the shape of a mortar by etching and performing high selectivity anisotropic etching of [the] a leading end of [the] said truncated conic body [in the shape of a mortar from the top surface to the bottom of the truncated body] to form [the] a truncated conic body having an annular leading end.

9. (Amended) A method for manufacturing a semiconductor device, comprising:

[forming an impurity precipitation region by] introducing [an] a first impurity into a predetermined position of a semiconducting material substrate or a semiconducting material layer, to obtain a semiconducting material substrate having an impurity precipitation region or a semiconducting material layer having an impurity precipitation region;

performing high selectivity anisotropic etching of [the] said semiconducting material

substrate having said impurity precipitation region or [the] of said semiconducting material layer [with the] having said impurity precipitation region [used as a micro mask], to thereby form a conic body;

wherein said impurity precipitation region is used as a micro mask during said anisotropic etching;

wherein said micro mask is a top of an etching exposure surface on which said anisotropic etching is performed and on which said conic body is formed [the top of which is the micro mask on an etching exposure surface of the material substrate or the material layer,];

forming an embedding layer on [the] said etching exposure surface [so] to obtain an embedded [embed the] conic body[,];

etching [the] said embedding layer [so] to etch [the] a top of [the] said embedded conic body[,]; and

performing high selectivity anisotropic etching of [the] a top surface of the conic body exposed to the surface into the shape of a mortar extending toward the bottom of the conic body to thereby form [the] a truncated conic body having an annular leading end.

10. (Amended) A semiconductor device, comprising:

a conic body formed on a semiconducting material substrate or a semiconducting material layer[,];

wherein said [the] conic body [having] has a radius of curvature of several to [ten or more] about 15 nm in the vicinity of its leading end or a diameter of about 10 nm to 30 nm in the vicinity of its leading end, and an aspect ratio of about 10 or more.

11. (Amended) A semiconductor device, comprising:

a truncated conic body formed on a semiconducting material substrate or a

semiconducting material layer[,];

wherein the truncated conic body [having] has a radius of curvature of several to [ten or] more than 10 nm in the vicinity of its leading end or a diameter of about several to 30 nm in the vicinity of its leading end, and an aspect ratio of about 10 or more, and an annular shape at its leading end with [the] a center of [the] a top surface partly removed.

12. (Amended) [A] The semiconductor device according to claim 11, wherein the truncated conic body has its leading end removed in the shape of a mortar from [the] a top face toward the bottom of the truncated conic body to form [the] an annular shape at the leading end.

13. (Amended) A single electron semiconductor device for controlling propagation of a single electron or a small number of electrons, comprising:

a silicon needle conic body protruded on a substrate as at least a part of a propagation passage for [the] said single electron or [the] said small number of electrons.

14. (Amended) [A] The device according to claim 13, further comprising:

a source region and a drain region closely disposed on [the] a side of [the] said silicon needle conic body with [the] said silicon needle conic body intervened therebetween[,];

wherein [the] said silicon needle conic body is used as a quantum dot[,]; and

wherein between the silicon needle conic body and the source region, between the silicon needle conic body and the drain region, between the source and drain regions, and a space between the silicon needle conic bodies where the silicon needle conic body is formed in multiple numbers, said silicon needle conic body is used as a small tunnel junction to control the propagation of a single or a small number of electrons between the source region and the drain region.

15. (Amended) [A] The single electron semiconductor device according to claim 13,

further comprising:

a potential control electrode for controlling [the] a potential in the conic body disposed around the side face of the silicon needle conic body[,];

wherein the propagation of [a] said single electron or [a] said small number of electrons is controlled between the vicinity of the bottom and the vicinity of the leading end of the silicon needle conic body by the potential control by the potential control electrode.

16. (Amended) [A] The single electron semiconductor device according to claim 13, further comprising:

a potential control electrode for controlling [the] a potential in the conic body disposed around the side face of the silicon needle conic body[,];

wherein the vicinity of the side face of the silicon needle conic body is depleted by the potential control [by the potential control] electrode to form a quantum wire region at [the] a core of the silicon needle conic body.

17. (Amended) [A] The device according to claim 16, wherein the silicon needle conic body has a conic shape with a radius of curvature of several to [ten or] more than 10 nm in the vicinity of its leading end or a diameter of about 10 nm to 30 nm in the vicinity of its leading end, and an aspect ratio of about 10 or more.

18. (Amended) [A] The device according to claim 16, wherein[:] the silicon needle conic body has a truncated conic body with a radius of curvature of several to [ten or] more than 10 nm in the vicinity of its leading end or a diameter of about 10 nm to 30 nm in the vicinity of its leading end, and an aspect ratio of about 10 or more[,]; and

wherein a [the] leading end of the truncated conic body has an annular shape with its center partly removed.

19. (Amended) A single electron semiconductor device for controlling propagation

of a single electron or a small number of electrons, comprising:

[a] silicon needle conic [body] bodies protruded on a substrate, and

a conducting material layer formed on the substrate [so] to bury at least the lower portions of the silicon needle conic bodies[,];

wherein[:] peripheral regions of the silicon needle conic bodies of the conducting material layer [are functioned] function as quantum dots and small tunnel junctions to control the propagation of [a] said single electron or [a] said small number of electrons in [the] a plane direction of the conducting material layer.

20. (Amended) [A] The single electron semiconductor device according to claim 19, wherein[:] each of the silicon needle conic [body] bodies is closely formed in multiple numbers [so] to be arranged in a breadth direction of the conducting material layer[,]; and

wherein the conducting material layer in a region intervened between two adjacent silicon needle conic bodies functions as the quantum dot and [the] a minute channel.

21. (Amended) [A] The single electron semiconductor device according to claim 19, wherein[:] each of the silicon needle conic [body] bodies is closely formed in multiple numbers in a direction along[the] an end of the conducting material layer[,];

wherein the conducting material layer which is in a region intervened between two adjacent silicon needle conic bodies functions as the quantum dot[,]; and

wherein the conducting material layer which is in a region intervened between the [plurality of arranged] silicon needle conic bodies and [the] an end of the conducting material layer functions as [the] a small tunnel junction.

22. (Amended) [A] The single electron semiconductor device according to claim 19, wherein[:] each of the silicon needle conic [body] bodies is closely formed in multiple numbers in a direction along [the] an end of the conducting material layer[,];

a depletion layer is formed in the conducting material layer in the peripheral region having the silicon needle conic body at [the] a center[,]; and

a quantum dot and a small tunnel junction are formed in a region between [the] a depletion layer end in the conducting material layer and [the] said end of the conducting material layer.

23. (Amended) [A] The device according to claim 19, wherein the silicon needle conic body has a radius of curvature of several to [ten or] more than 10 nm in the vicinity of its leading end or a diameter of about 10 nm to 30 nm in the vicinity of its leading end, and an aspect ratio of about 10 or more.

24. (Amended) [A] The device according to claim 19, wherein[:] the silicon needle conic body has a truncated conic body with a radius of curvature of several to [ten or] more than 10 nm in the vicinity of its leading end or a diameter of about 10 nm to 30 nm in the vicinity of its leading end, and an aspect ratio of about 10 or more[,]; and

wherein a [the] leading end of the truncated conic body has an annular shape with its center partly removed.

25. (Amended) A semiconductor memory for storing information by accumulating electric charges in a capacitor configuring each memory unit, comprising:

a needle of silicon crystal formed in each memory unit, and a capacitor having the side face of the needle as one of electrodes.

26. (Amended) [A] The semiconductor memory according to claim 25, wherein a switching transistor is formed on a part of the silicon crystal needle to supply the capacitor with electric charges.

27. (Amended) [A] The semiconductor memory according to claim 26, wherein the switching transistor is formed at [the] a base of the silicon crystal needle, and the capacitor is

formed at [the] a leading end.

28. (Amended) [A] The semiconductor memory according to claim 26, wherein the switching transistor is formed at [the] a leading end of the silicon crystal needle, and the capacitor is formed below the switching transistor.

29. (Amended) [A] The device according to claim 25, wherein the silicon crystal needle has a conic shape with a radius of curvature of several to [ten or] more than 10 nm in the vicinity of its leading end or a diameter of about 10 ran to 30 nm in the vicinity of its leading end, and an aspect ratio of about 10 or more.

30. (Amended) A method for manufacturing a single electron semiconductor device for controlling propagation of a single electron or a small number of electrons, comprising:

forming an impurity precipitation region in a single-crystal silicon substrate or a single-crystal silicon layer, to obtain a single-crystal silicon substrate having an impurity precipitation region or a single-crystal silicon layer having an impurity precipitation region;

performing high selectivity anisotropic etching of [the] said single-crystal silicon substrate having said impurity precipitation region or of said [the] single-crystal silicon layer [with the] having said impurity precipitation region [used as a micro mask] to thereby form a silicon needle conic body;

wherein said impurity precipitation region is used as a micro mask during said anisotropic etching; and

wherein [the] a top of [which is the] said silicon needle conic body is said micro mask[,]; and

using the silicon needle conic body as at least a part of a propagation route of the single electron or the small number of electrons of the single electron semiconductor device.

31. (Amended) A method for manufacturing a single electron semiconductor device

for controlling propagation of a single electron or a small number of electrons, comprising:

forming an impurity precipitation region in a single-crystal silicon substrate or a single-crystal silicon layer, to obtain a single-crystal silicon substrate having an impurity precipitation region or a single-crystal silicon layer having an impurity precipitation region;

performing high selectivity anisotropic etching of [the] said single-crystal silicon substrate having said impurity precipitation region or of said [the] single-crystal silicon layer [with the] having said impurity precipitation region [used as a micro mask] to thereby form a silicon needle conic body;

wherein said impurity precipitation region is used as a micro mask during said anisotropic etching; and

wherein [the] a top of [which is the] said silicon needle conic body is said micro mask[,];

forming a conducting material layer on[the] said single-crystal silicon substrate [so] to bury [the] said silicon needle conic body [and] or at least a lower portion of the silicon needle conic body, and

[functioning the] wherein a peripheral region of the silicon needle conic body of the conducting material layer functions as a quantum dot and a small tunnel junction to control the propagation of [a] said single electron or [a] said small number of electrons in [the] a planar direction of the conducting material layer.

32. (Amended) A semiconductor memory for storing information, comprising:

an impurity precipitation region in a single-crystal silicon substrate or a single-crystal silicon layer,

a silicon crystal needle conic body formed in each memory unit on [the] said single-crystal silicon substrate by subjecting [the] said single-crystal silicon substrate having said

impurity precipitation region or [the] said single-crystal silicon layer having said impurity precipitation region to high selectivity anisotropic etching;

wherein said [with the] impurity precipitation region is used as a micro mask[,];

wherein said [the silicon precipitation region having] single-crystal silicon substrate or said single-crystal silicon layer have [the] said micro mask at [the] a top[,]; and

a capacitor having [the] a side face of the silicon crystal needle as one of electrodes[,];

wherein information is stored by accumulating electric charges into [the] said capacitor.

33. (Amended) A semiconductor device, comprising:

a conic body formed on a semiconducting material substrate or a semiconducting material layer;

wherein said conic body has a radius of curvature of several to more than 10 nm in the vicinity of its leading end or a diameter of about 10 nm to 30 nm in the vicinity of its leading end, and an aspect ratio of about 10 or more;

wherein said [The] semiconductor device [according to Claim 10, which] is a single electron semiconductor device for controlling propagation of a single electron or a small number of electrons;

wherein said conic body is a silicon needle conic body protruded on said substrate as at least a part of a propagation passage for the single electron or the small number of electrons.

35. (Amended) A semiconductor device, comprising:

a conic body formed on a semiconducting material substrate or a semiconducting material layer;

wherein said conic body has a radius of curvature of several to more than 10 nm in the

vicinity of its leading end or a diameter of about 10 nm to 30 nm in the vicinity of its leading end, and an aspect ratio of about 10 or more;

wherein said [The] semiconductor device [according to Claim 10, which] is a single electron semiconductor device for controlling propagation of a single electron or a small number of electrons;

wherein said conic body is a silicon needle conic body protruded on said substrate;

wherein said semiconductor device further comprises a conducting material layer formed on said substrate to bury at least a lower portion of the silicon needle conic [bodies] body;

wherein peripheral regions of the silicon needle conic bodies of the conducting material layer are functioned as quantum dots and small tunnel junctions to control the propagation of a single electron or a small number of electrons in [the] a plane direction of the conducting material layer.

36. (Amended) The semiconductor device according to Claim 11, which is a single electron semiconductor device for controlling propagation of a single electron or a small number of electrons;

wherein said conic body is a silicon needle conic body protruded on said substrate;

wherein said semiconductor device further comprises a conducting material layer formed on said substrate to bury at least a lower portion of the silicon needle conic [bodies] body;

wherein peripheral regions of the silicon needle conic bodies of the conducting material layer are functioned as quantum dots and small tunnel junctions to control the propagation of a single electron or a small number of electrons in [the] a plane direction of the conducting material layer.

37. (Amended) A semiconductor device, comprising:

a conic body formed on a semiconducting material substrate or a semiconducting material layer;

wherein said conic body has a radius of curvature of several to more than 10 nm in the vicinity of its leading end or a diameter of about 10 nm to 30 nm in the vicinity of its leading end, and an aspect ratio of about 10 or more;

wherein said [The] semiconductor device [according to Claim 10, which] is a semiconductor memory for storing information by accumulating electric charges in a capacitor configuring each memory unit,

wherein said semiconductor memory further comprises a needle of silicon crystal formed in each memory unit, and a capacitor having the side face of the needle as one of electrodes.

38. (Amended) A semiconductor device, comprising:

a conic body formed on a semiconducting material substrate or a semiconducting material layer;

wherein said conic body has a radius of curvature of several to more than 10 nm in the vicinity of its leading end or a diameter of about 10 nm to 30 nm in the vicinity of its leading end, and an aspect ratio of about 10 or more;

wherein said [The] semiconductor device [according to Claim 10, which] is a semiconductor memory for storing information,

wherein said semiconductor memory comprises

an impurity precipitation region in a single-crystal silicon substrate or a single-crystal silicon layer,

said conic body which is a silicon crystal needle conic body formed in each memory

unit on the substrate by subjecting the silicon substrate or the silicon layer to high selectivity anisotropic etching with the impurity precipitation region used as a micro mask, the silicon precipitation region having the micro mask at [the] a top, and

a capacitor having [the] a side face of the silicon crystal needle as one of electrodes, wherein information is stored by accumulating electric charges into the capacitor.--

Claims 39-48. (New)